Please replace the paragraphs on page 8, beginning on line 18, through page 9, line 12, with the following:

--capacitor structures, each having a first gate insulating film formed on a semiconductor substrate of a first conductivity type, and a first gate electrode formed on the first gate insulating film; and

electric fuse elements, each having a second gate insulating film formed on the semiconductor substrate and having an impurity concentration higher than that of the first gate insulating film, and a second gate electrode formed on the second gate insulating film, wherein information is written in the electric fuse element depending on whether the second gate insulating film is dielectrically broken down, and a writing voltage of the electric fuse element is determined by dielectric breakdown resistance of the second gate insulating film which depends on the impurity concentration of the second gate insulating film; and

an impurity diffusion layer of a second conductivity type, which is formed in at least a portion of the semiconductor substrate, the impurity diffusion layer being paired with the second gate electrode and serving as one electrode of the electric fuse element.--.

Please delete the paragraphs on page 9, beginning on line 13, through page 10, line 3.

Please replace the paragraph on page 10, beginning on line 4 with the following:

--A method for fabricating an electric fuse according to an aspect of the present invention comprises:--

Please delete the paragraphs on page 10, beginning on line 15, through page 13, line 6.

Please delete the paragraph on page 13, beginning on line 8.

Please replace the paragraph on page 16, beginning on line 22 with the following:

--Thereafter, an impurity diffusion layer of a MOS transistor and an interlayer insulating film covering the MOS transistor are formed by the known technique. As a result, a semiconductor device is completed. In the semiconductor device as shown in FIG. 3C, a fuse capacitor comprising the silicon substrate 30, the gate insulating film 32b doped with the impurity and the gate electrode 33 forms an anti-fuse.

Please replace the paragraph on page 19, beginning on line 2 with the following:

--Thereafter, a resist 50-2 is formed on the silicon substrate 30, and then patterned to expose only a portion of the peripheral region by means of lithography. Then, as shown in FIG. 4B, an n-type impurity is ion-injected. The acceleration voltage at the ion injection is adjusted so that the impurity ions can be implanted into the gate insulating film 32a and the silicon substrate 30 through the tungsten film 33b and the polycrystalline silicon film 33a. Through this step, a gate insulating film 32b doped with the impurity is formed in the peripheral region A4, and an n-type impurity diffusion layer 51 is formed in the silicon substrate 30. As described above, the gate electrode 33 in the peripheral region A4 is displaced from the element region. Therefore, the impurity diffusion layer 51 formed in the silicon substrate 30 includes two impurity diffusion layers 51a and 51b of different depths. In other words, due to the ions passing through the gate electrode 33, the impurity diffusion layer 51b formed immediately under the gate electrode 33 is shallower than the impurity diffusion layer 51a, which is not covered by the gate electrode 33. --.

Please replace the paragraph on page 35, beginning on line 1 with the following:

--In the embodiments described above, the anti-fuse utilizes a part of the cell capacitor or the MOS transistor of a DRAM. However, the embodiment of the present invention is to control the dielectric breakdown resistance by introducing an impurity into the insulating film of the anti-fuse. Therefore, the embodiment of the present invention is not limited to the structures of the first to fifth embodiments. Other structures of the embodiments will be described below.--

Please replace the paragraph on page 35, beginning on line 14 with the following:

--FIG. 9A shows an anti-fuse using an interlayer insulating film. As shown in FIG. 9A, a polycrystalline silicon film 33a and a tungsten film 33b, serving as a gate electrode 33, are formed on a gate insulating film 32a, which is formed on a silicon substrate 30. An interlayer insulating film 52 is formed on the tungsten film 33b. A metal wiring layer 54 including a barrier metal layer 54a and a metal layer 54b is formed on the interlayer insulating film 52. This structure constitutes an anti-fuse in which the gate electrode 33 and the metal wiring layer 54 serve as capacitor electrodes and the interlayer insulating film 52 serves as a capacitor insulating film. The dielectric breakdown resistance, i.e., the writing voltage, of the anti-fuse can be controlled by ion-injecting an impurity into the interlayer insulating film 52 serving as the capacitor insulating film.--

Please replace the paragraph on page 36, beginning on line 5 with the following:

--FIG. 9B shows an anti-fuse using a gate sidewall insulating film. As shown in FIG. 9B, a gate electrode 33 is formed on a silicon substrate 30 with a gate insulating film 32a interposed

therebetween. A gate sidewall insulating film 55 covering the gate electrode 33 is provided. A metal wiring layer 56 abuts on the gate sidewall insulating film 55. This structure forms an anti-fuse in which the gate electrode 33 and the metal wiring layer 56 serve as capacitor electrodes and the gate sidewall insulating film 55 serves as a capacitor insulating film. The dielectric breakdown resistance, i.e., the writing voltage, of the anti-fuse can be controlled by ion-injecting an impurity into the gate sidewall insulating film 55 serving as the capacitor insulating film.--

Please replace the paragraph on page 36, beginning on line 20 with the following:

--FIG. 9C shows an anti-fuse using an insulating film interposed between metal wiring layers. As shown in FIG. 9C, two metal wiring layers 57 are buried in an interlayer insulating film 52. An anti-fuse includes the metal wiring layers 57 serving as capacitor electrodes, and the portion of the interlayer insulating film 52 located between the two wiring layers 57, which serves as a capacitor insulting film. The dielectric breakdown resistance, i.e., the writing voltage, of the anti-fuse can be controlled by ion-injecting an impurity into the portion of the interlayer insulating film 52 located between the two metal wiring layers 57. --.